IN THE CLAIMS

Please amend the claims as follows:

Claim 1 (Currently Amended): A CMOS image sensor ~~according to an embodiment of the present invention comprises~~ comprising:

a plurality of unit cells arranged in the row and column directions at [[a]] predetermined ~~pitch~~ pitches of ph0 and pv0 respectively in a two-dimensional plain forming a matrix, ~~which include~~ each of the unit cells including:

a first and a second photoelectric conversion element, each of which corresponds to a pixel,

a first and a second transfer transistor for transferring charges stored by the photoelectric conversion elements [[at]] to their common floating ~~junctions~~ junction,

a reset ~~transistors~~ transistor for resetting the potential of the floating ~~junctions~~ junction,

a driver ~~transistors~~ transistor whose output potential is controlled by the potential of the floating ~~junctions~~ junction, and

an address ~~transistors~~ transistor for selectively driving the driver ~~transistors~~ transistor;

reset drain voltage lines provided in the column direction of the matrix arrangement for resetting the potential of the common floating junctions included in the unit cell belonging to each column of the matrix arrangement;

first transfer lines provided in the row direction of the matrix arrangement for controlling the first transfer transistor included in the unit cell belonging to each row;

second transfer lines in the row direction of the matrix arrangement for controlling the second transfer transistors included in the unit cells belonging to each row of the matrix arrangement;

signal output lines provided in the column direction of the matrix arrangement to which the output voltages of the driver transistors included in the unit cells belonging to each column of the matrix arrangement are supplied, and

address lines provided in the row direction of the matrix arrangement for selectively driving the driver transistors included in the unit cell belonging to each row, wherein

the first and the second photoelectric conversion elements are spaced by ph0/2 and pv0/2 to each other in the horizontal and vertical directions, thereby being arranged in an oblique direction in relation to the row or column directions of the matrix, and

the first and the second transfer transistors, the floating junction, the reset transistor, the driver transistor or the address transistor included in each of the unit cells are placed in areas surrounded by adjacent unit cells.

Claim 2 (Original): A CMOS image sensor according to claim 1, wherein a first pixel line composed of the first photoelectric conversion element included in the unit cells belonging to each row of the matrix arrangement and a second pixel lines composed of the second photoelectric conversion element included in the unit cells are independently read respectively by the first and second transfer lines.

Claim 3 (Original): A CMOS image sensor according to claim 2, wherein the first pixel lines and the second pixel lines are read by switching the first and second transfer transistors by the first and second transfer lines.

Claim 4 (Original): A CMOS image sensor according to claim 3, wherein the driver transistors and the address transistors which are included in the respective unit cells are connected in series, wherein the first and second photoelectric conversion elements are

connected to gate electrodes of the driver transistors via the first and second transfer transistors, and wherein source electrodes of the reset transistors are connected to the gate electrodes of the driver transistors.

Claim 5 (Original): A CMOS image sensor according to claim 4, wherein the first and second photoelectric conversion elements are photodiodes.

Claim 6 (Canceled).

Claim 7 (Currently Amended): A CMOS image sensor according to claim [[6]] 5, wherein the unit cells are formed as an integrated circuit on a semiconductor substrate and the first and second photodiodes arranged in the oblique direction share the floating junction area, the reset drain area, the reset transistors, the driver transistors, the address transistors, the junction area between the driver transistors and the address transistors and the diffusion area at the connecting portion between the driver transistors and the signal output line, thereby reading signals of the first pixel row and the second pixel row independently.

Claim 8 (Currently Amended): A CMOS image sensor ~~according to an embodiment of the present invention comprises~~ comprising:

a plurality of unit cells arranged in the row and column directions at a predetermined pitch of ph0 and pv0, respectively, in a two-dimensional plain forming a matrix, each of the unit cells including: ~~which include~~

a first and a second photoelectric conversion element, each of which corresponds to a pixel,

a first and a second transfer transistor for transferring charges stored by the photoelectric conversion elements ~~at~~ to their common floating junctions,

a reset ~~transistors~~ transistor for resetting the potential of the floating junction ~~junctions~~,

a driver ~~transistors~~ transistor whose output potential is controlled by the potential of the floating junction ~~junctions~~, and

an address ~~transistors~~ transistor for selectively driving the driver ~~transistors~~ transistor;

reset drain voltage lines provided in the column direction of the matrix arrangement for resetting the potential of the common floating junctions included in the unit cell belonging to each column of the matrix arrangement;

first transfer lines provided in the row direction of the matrix arrangement for controlling the first transfer transistor included in the unit cell belonging to each row;

second transfer lines in the row direction of the matrix arrangement for controlling the second transfer transistors included in the unit cells belonging to each row of the matrix arrangement;

first signal output lines provided in the column direction of the matrix arrangement to which the output voltages of the driver transistors included in the unit cells arranged in the odd numbered rows are supplied;

second signal output lines provided in the column direction of the matrix arrangement to which the output voltages of the driver transistors included in the unit cells arranged in the even numbered rows are supplied; and

address lines provided in the row direction of the matrix arrangement for selectively driving the driver transistors included in the unit cell belonging to each row [[;]], wherein

the first and the second photoelectric conversion elements are spaced by ph0/2 and pv0/2 to each other in the horizontal and vertical directions, thereby being arranged in an oblique direction in relation to the row or column directions of the matrix,

the first and the second transfer transistors, the floating junction, the reset transistor, the driver transistor or the address transistor included in each of the unit cells are placed in areas surrounded by adjacent unit cells, and

image signals of the pixel arrays composed of the photoelectric conversion elements included in the unit cells arranged in the neighboring two columns are read simultaneously using the first and second signal output lines.

Claim 9 (Original): A CMOS image sensor according to claim 8, wherein the adjacent pixel lines, which are read simultaneously, are a pixel row formed by the second photoelectric conversion elements included in the unit cell belonging to the first row and a pixel row formed by the first photoelectric conversion element included in the unit cell belonging to the second row, thereby simultaneously read the image signals of the pixel of adjacent tow rows into the first and second signal output lines by respectively supplying the same transfer pulse to the second transfer line provided for the unit cell belonging to the first row and the first transfer line provided for the unit cell belonging to the second row.

Claim 10 (Original): A CMOS image sensor according to claim 9, a gate of the second transfer transistor included in the unit cell belong to the first row and a gate of the first transfer transistor included in the unit cell belong to the second row are connected to each other.

Claim 11 (Original): A CMOS image sensor according to claim 10, wherein the first pixel row composed of the first photoelectric conversion element included in the unit cells belonging to the respective rows of the matrix arrangement and the second pixel row composed of the second photoelectric conversion element included in the unit cells are independently read respectively by the first and second transfer lines.

Claim 12 (Original): A CMOS image sensor according to claim 11, wherein the first pixel row and the second pixel row are read by switching the first and second transfer transistors by the first and second transfer lines.

Claim 13 (Original): A CMOS image sensor according to claim 12, wherein the driver transistors and the address transistors, which are included in the unit cells are connected in series, wherein the first and second photoelectric conversion elements are connected to gate electrodes of the driver transistors via the first and second transfer transistors, and wherein source electrodes of the reset transistors are connected to the gate electrodes of the driver transistors.

Claim 14 (Original): A CMOS image sensor according to claim 13, wherein the first and second photoelectric conversion elements are photodiodes.

Claim 15 (Canceled).

Claim 16 (Currently Amended): A CMOS image sensor according to claim [[15]] 14, wherein the unit cells are formed as an integrated circuit on a semiconductor substrate and wherein the first and second photodiodes arranged in the oblique direction share the floating

junction area, the reset drain area, the reset transistors, the driver transistors, the address transistors, the junction area between the driver transistors and the address transistors, and the diffusion area at the connecting portion between the driver transistors and the signal output line,

thereby reading signals of the first pixel row and the second pixel row independently.

Claim 17 (Original): A CMOS image sensor according to claim 1, wherein among unit cells arranged in adjacent two rows of the matrix arrangement, a gate of the address transistor included in the unit cell arranged in the first row and a gate of the reset transistor included in the unit cell arranged in the second row are connected, and while an image signal from the second photoelectric conversion element included in the unit arranged in the first row is being read, the floating junction included in the unit cell arranged in the second row to be read next is reset, thus an image signal from the first photoelectric conversion element included in the unit cell arranged in the second row can be read.

Claim 18 (Original): A CMOS image sensor according to claim 17, wherein a first pixel row composed of the first photoelectric conversion element included in the unit cell belonging to each row of the matrix arrangement and a second pixel row composed of the second photoelectric conversion element included in the unit cell are independently read by the first and second transfer lines.

Claim 19 (Original): A CMOS image sensor according to claim 18, wherein the first pixel row and the second pixel row are read by switching the first and second transfer transistors by the first and second transfer lines.

Claim 20 (Original): A CMOS image sensor according to claim 19, wherein the driver transistors and the address transistors which are included in the unit cells are connected in series, and the first and second photoelectric conversion elements are connected to gate electrodes of the driver transistors via the first and second transfer transistors, and source electrodes of the reset transistors are connected to the gate electrodes of the driver transistors.

Claim 21 (Original): A CMOS image sensor according to claim 19, wherein the first and second photoelectric conversion elements are photodiodes.

Claim 22 (Canceled).

Claim 23 (Original): A CMOS image sensor according to claim 21, wherein unit cells are formed as an integrated circuit on a semiconductor substrate and the first and second photodiodes arranged in the oblique direction share the floating junction area, the reset drain area, the reset transistors, the driver transistors, the address transistors, the junction area between the driver transistors and the address transistors and the diffusion area at the connecting portion between the driver transistors and the signal output line, thereby read signals of the first pixel row and the second pixel row independently.